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Support for the Amendments

Support for the present amendments can be found throughout the specification, claims and figures as originally filed. Without being limited to such exemplary passages and/or other disclosures, support for the amendments to claim 1 and for new claims 21-22 can be found in claim 1 as originally filed, FIGS. 1-3, and in the specification on page 2, lines 7-8, page 3, lines 21-31, and page 4, lines 26-29. Thus, no new matter is introduced by the present Amendment.

Remarks

Applicant thanks Examiner Nguyen for the courteous and helpful discussion held with the undersigned practitioner on October 25, 2005. However, the combination of claims 1, 19 and 20 has been presented as new claim 22, and claim 1 has been amended to include the limitation of claim 19 and the width of the opening in the photoresist, as discussed on October 25, 2005. Applicant also submits herewith the Declaration of Kang-Hyun Lee (as generally discussed on October 25, 2005), explaining the unexpected results provided by the presently claimed invention. The following remarks shall further summarize and expand upon topics discussed.

The present invention relates to a method for fabricating a metal line of a semiconductor device. The method generally forms a photoresist pattern on a metal layer, where the photoresist has a thickness of less than 9000 Å; forming a buffer layer on the photoresist pattern, including in an opening in the photoresist pattern; and removing the metal layer at a lower side of the opening by dry etching to form a plurality of metal lines. In one aspect, the photoresist pattern has an opening of less than or equal to 0.26 µm width (amended Claim 1 above), and in a related aspect, a ratio of the photoresist thickness to the width of the opening is less than about 3.5 (new Claim 22 above). The method shows unexpected improvements in defect reduction relative to otherwise identical methods in which no buffer layer is formed on the photoresist pattern and either:

- (i) The photoresist has a thickness greater than 9000 Å and a ratio of the photoresist thickness to the width of the opening is greater than about 3.5; or

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- (ii) The photoresist has a thickness less than 9000 Å (see, e.g., paragraph 4 of the Declaration of Kang-Hyun Lee, submitted herewith).

This result is neither disclosed nor suggested by the cited references.

The Rejections of the Claims under 35 U.S.C. § 103(a)

The rejection of Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over Narita et al. (hereinafter, "Narita") in view of Chung et al. (hereinafter, "Chung") is respectfully traversed.

Narita disclose a dry etching method for use in patterning stacked metal films containing aluminum as the base component and a thin film including at least one of titanium and titanium nitride. In this method, the thin film is dry-etched using a first etching gas composition for preventing the metal film from being processed. The metal film is then dry-etched using a second etching gas composition other than the first etching gas (Abstract).

The method of Narita intends to provide a dry etching method capable of patterning a stacked film such that the thin film is formed vertically and the metal film is prevented from being side-etched (col. 2, ll. 47-53) and/or reduce a pattern transfer difference in a stacked film (col. 3, ll. 1-4). As the Examiner correctly recognizes, Narita do not disclose forming a buffer layer as claimed (see, e.g., page 3, lines 6-7 of the Office Action).

Chung discloses a semiconductor manufacturing method that includes defining a substrate, depositing a polysilicon layer over the substrate, depositing a layer of photoresist over the polysilicon layer, patterning and defining the photoresist layer, depositing a layer of inorganic material over the patterned and defined photoresist layer where the layer of inorganic material is conformal and photo-insensitive, and anisotropically etching the layer of inorganic material and the layer of semiconductor material (Abstract). While Chung seeks to enhance the etching resistance of a patterned photoresist layer (col. 1, ll. 37-39), Chung appears to be silent with regard to any defect reduction effects of forming the layer of inorganic material over the patterned and defined photoresist layer. Accordingly, Chung cannot suggest the observed

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improvements in defect reduction provided by the present method as a result of forming a buffer layer on a photoresist pattern.

For example, step e) in the present claims 1 and 22 recites "selectively removing the metal layer at a lower side of the opening by dry etching to form a plurality of metal lines." In processes used to manufacture commercial semiconductor devices, to form a plurality of metal lines successfully, gaps between adjacent metal lines are formed without defects that cause a short circuit between the adjacent metal lines (see, e.g., paragraph 5 of the Lee Declaration, submitted herewith).

In processes used to manufacture commercial semiconductor devices in which a critical dimension between adjacent metal lines is $0.26\text{ }\mu\text{m}$ or less, a problem arises when the photoresist has a thickness greater than $9000\text{ }\text{\AA}$. In this case, the openings in the photoresist have an aspect ratio (i.e., the ratio of the photoresist thickness to the width of the opening) of greater than about 3.5. In other words, since $9000\text{ }\text{\AA}/2600\text{ }\text{\AA}$ ($0.26\text{ }\mu\text{m}$) is about 3.5 (using 2 significant digits), a photoresist thickness of $> 9000\text{ }\text{\AA}$ divided by a width of $0.26\text{ }\mu\text{m}$ leads to an aspect ratio of $>$ about 3.5 (see paragraphs 6-7 of the Lee Declaration, submitted herewith).

The relationship between the aspect ratio of the openings in the photoresist and the width of the openings in the photoresist is direct and quite clear, as the statement in paragraph 7 of the Lee Declaration establishes. In other words, the width of the opening times the aspect ratio equals the height of the photoresist. Therefore, the unexpected results described in the accompanying Lee Declaration for a method that forms a buffer layer on a photoresist pattern on a metal layer, where the photoresist has a thickness of less than $9000\text{ }\text{\AA}$, and a ratio of the photoresist thickness to the width of an opening in the photoresist is less than about 3.5 (new Claim 22 above), are applicable to a photoresist pattern having a thickness of less than $9000\text{ }\text{\AA}$ and an opening of less than or equal to $0.26\text{ }\mu\text{m}$ width (amended Claim 1 above).

When the openings in the photoresist have an aspect ratio $>$ about 3.5, the aspect ratio of the gap formed between adjacent metal lines having relatively thick photoresist thereon increases. This increase results in an increased likelihood of the formation of metal "stringers" or other defects at the bottom of the gaps between the resulting metal lines that result in a short

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circuit between adjacent metal lines. In the case where the photoresist has a thickness greater than 9000 Å and the openings in the photoresist have an aspect ratio > about 3.5, the increased likelihood of metal "stringers" or other short circuit-causing defects is unacceptably high for a commercial manufacturing process (see paragraphs 8-9 of the accompanying Lee Declaration).

One possible solution to this metal "stringer" problem is to reduce the photoresist thickness to less than 9000 Å. (In a commercial semiconductor manufacturing process, one generally cannot reduce the metal layer thickness without adversely affecting performance of the manufactured semiconductor devices.) However, in many commercial semiconductor manufacturing processes, a thickness of less than 9000 Å for a conventional photoresist may not be sufficient to dry etch the metal layer under the photoresist (see the last step in claims 1 and 22 above; also see paragraph 10 of the accompanying Lee Declaration).

Typical conditions for dry etching a metal layer in commercial semiconductor manufacturing processes are generally not sufficiently selective with respect to the photoresist to ensure that an adequate amount of photoresist remains over the metal layer to prevent inadvertent etch damage to the top of the metal layer. Thus, when the photoresist thickness is less than 9000 Å in commercial CMOS semiconductor manufacturing processes, there is an increased likelihood of damage to the upper surfaces of the resulting metal lines that can degrade performance of the resulting semiconductor devices and/or adversely affect subsequent processing (e.g., anti-reflective coatings formed at or on the upper surface of the metal lines may have unacceptable anti-reflective properties). In this case, the increased likelihood of dry etch damage to the upper surface of the metal lines is unacceptably high for a commercial semiconductor manufacturing process (see paragraphs 11-12 of the accompanying Lee Declaration).

To solve these "metal stringer" and dry etch damage problems, the present method (e.g., as recited in claim 22 above) first forms a photoresist pattern on the metal layer, where the photoresist has a thickness of less than 9000 Å and a ratio of the photoresist thickness to the width of an opening in the photoresist is less than about 3.5, then forms a buffer layer on the photoresist pattern, including in the opening (see paragraph 13 of the accompanying Lee

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Declaration). Alternatively, the present method may form a photoresist pattern having an opening of less than or equal to 0.26 μm width and a thickness of less than 9000 Å on the metal layer, then forms a buffer layer on the photoresist pattern, including in the opening (see amended claim 1 above).

The present method (as exemplified by claim 22 above) above reduces the likelihood of "metal stringer" (or other short circuit-causing) defects and any adverse effects from dry etch damage to an upper surface of metal lines to levels or values that are acceptable for commercial semiconductor manufacturing processes (see paragraph 14 of the accompanying Lee Declaration). Given the direct relationship between aspect ratio and width of an opening in a photoresist pattern as established by paragraph 7 of the accompanying Lee Declaration, the improvements provided by the present method (as exemplified by claim 22 above) are also applicable to a photoresist pattern having a thickness of less than 9000 Å and an opening of less than or equal to 0.26 μm width (see amended Claim 1 above).

One of ordinary skill in the art of semiconductor manufacturing would not understand or appreciate from reading the Narita and Chung patents that the present method (e.g., as recited in claim 22 above) would provide the observed improvements in defect reduction (i.e., from commercially unacceptable levels to commercially acceptable levels; see paragraph 15 of the accompanying Lee Declaration). Given the direct relationship between aspect ratio and width of an opening in a photoresist pattern as established by paragraph 7 of the Lee Declaration, the unexpected improvements provided by the present method (exemplified by claim 22 above) are also applicable to a photoresist pattern having a thickness of less than 9000 Å and an opening of less than or equal to 0.26 μm width (see amended Claim 1 above).

For example, Narita discloses a dry etching method for use in patterning stacked metal films containing aluminum as the base component and a thin film including at least one of titanium and titanium nitride (Abstract). The method of Narita intends to provide a dry etching method capable of patterning a stacked film such that the thin film is formed vertically, and the metal film is prevented from being side-etched (col. 2, ll. 47-53) and/or a pattern transfer

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difference is reduced in the stacked film (col. 3, ll. 1-4 of Narita; see also paragraph 16 of the accompanying Lee Declaration).

Narita teaches that the width of processed wiring usually becomes larger than that of a mask when a mask pattern is formed on the stacked film, and then the stacked film is processed by dry etching (col. 10, ll. 18-21). In such a case, it is likely that an interval (or gap) between wiring portions will be narrowed, and a short circuit will be caused easily between them (Narita, col. 10, ll. 21-24). This disclosure is consistent with the discussion in paragraphs 8-9 above regarding the "metal stringer" problem (see paragraph 17 of the accompanying Lee Declaration).

Narita further teaches that this problem is difficult to solve in miniaturized devices using conventional approaches (col. 10, ll. 35-36). For example, the wiring cannot be thinned because its resistance is increased, and accordingly, the photoresist mask pattern cannot be reduced in thickness (Narita, col. 10, ll. 36-41). Consequently, Narita teaches that the mask is narrowed and the photoresist mask aspect ratio is increased, resulting in a phenomenon in which the mask pattern is easy to physically fall when it is washed after development (col. 10, ll. 41-45). This disclosure is consistent with the discussion in paragraph 10 above regarding problems resulting from conventional solutions to the "metal stringer" problem (see paragraph 18 of the accompanying Lee Declaration).

Narita appears to be silent with regard to forming a buffer layer on a photoresist pattern. Accordingly, Narita cannot suggest the observed improvements in defect reduction provided by the present method (as recited in paragraph 3 of the accompanying Lee Declaration and claim 22 above) as a result of forming a buffer layer on a photoresist pattern (see paragraph 19 of the accompanying Lee Declaration). Given the direct relationship between aspect ratio and width of an opening in a photoresist pattern as established by paragraph 7 of the Lee Declaration, the deficiencies of Narita are also applicable to an identical method in which the photoresist has a thickness of less than 9000 Å and the photoresist pattern has an opening of less than or equal to 0.26 µm width (see amended Claim 1 above).

Chung discloses a semiconductor manufacturing method that includes defining a substrate, depositing a polysilicon layer over the substrate, depositing a layer of photoresist over

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the polysilicon layer, patterning and defining the photoresist layer, depositing a layer of inorganic material over the patterned and defined photoresist layer where the layer of inorganic material is conformal and photo-insensitive, and anisotropically etching the layer of inorganic material and the layer of semiconductor material (Abstract; see also paragraph 20 of the accompanying Lee Declaration).

While it is an object of the invention of Chung to enhance the etching resistance of a patterned photoresist layer (col. 1, ll. 37-39), Chung appears to be silent with regard to any defect reduction effects of forming the layer of inorganic material over the patterned and defined photoresist layer. Accordingly, Chung cannot suggest the observed improvements in defect reduction provided by the present method (recited in paragraph 3 of the accompanying Lee Declaration and claim 22 above) as a result of forming a buffer layer on a photoresist pattern. Given the direct relationship between aspect ratio and width of an opening in a photoresist pattern as established by paragraph 7 of the Lee Declaration, the deficiencies of Chung are also applicable to an identical method in which the photoresist has a thickness of less than 9000 Å and the photoresist pattern has an opening of less than or equal to 0.26 µm width (see amended Claim 1 above).

As a result, the observed improvements in defect reduction provided by the present method (e.g., as recited in paragraph 3 of the accompanying Lee Declaration and claim 22 above) are unexpected in view of the Narita and Chung patents. Given the direct relationship between aspect ratio and width of an opening in a photoresist pattern established by paragraph 7 of the Lee Declaration, the unexpected improvements provided by the present method (exemplified by claim 22 above) are also applicable to an identical method in which the photoresist has a thickness of less than 9000 Å and the photoresist pattern has an opening of less than or equal to 0.26 µm width (see amended Claim 1 above).

Consequently, both the present claims 1 and 22 provide improvements in defect reduction that are unexpected in view of the disclosures and teachings of Narita and Chung. As a result, the present claims 1 and 22 are fully patentable over Narita and Chung.

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Claims 2-20 all depend directly or indirectly from claim 1, and are therefore believed to be patentable for the same reasons as claim 1. Thus, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases for rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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